(PRIOR ART)
8 POINTS DFT

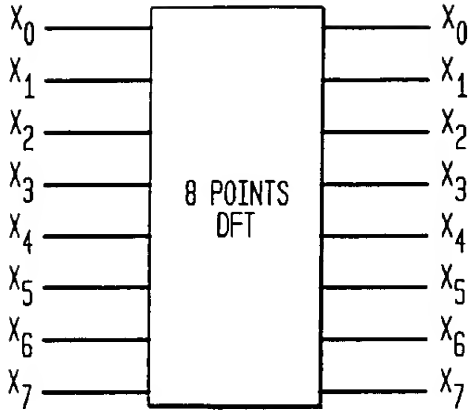


Fig 1A

(PRIOR ART)
8 POINTS DFT OBTAINED BY COMBINING TWO FOUR POINTS DFT

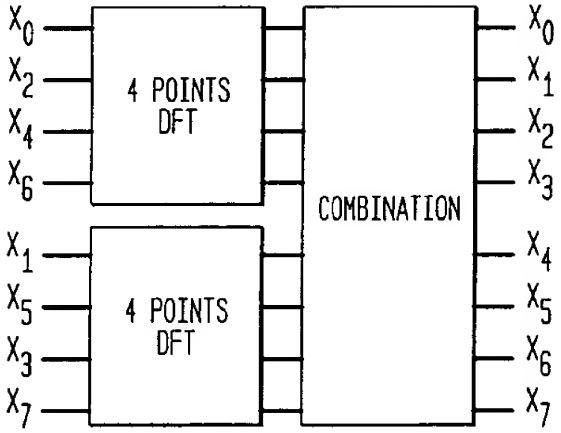


Fig 1B

(PRIOR ART)
8 POINTS DFT OBTAINED BY COMBINING FOUR TWO POINTS DFT

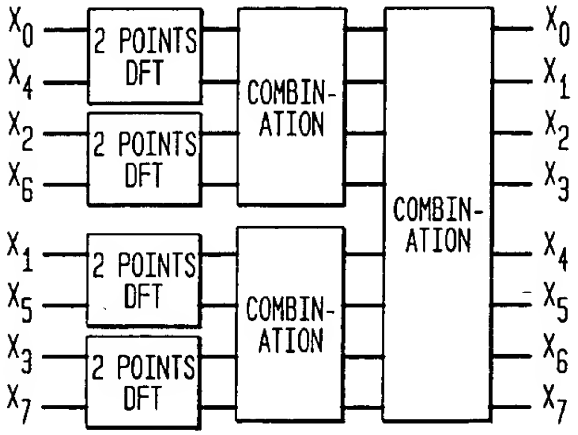


Fig 1C

(PRIOR ART)

DIT RADIX-2 BUTTERFLY COMPUTATION

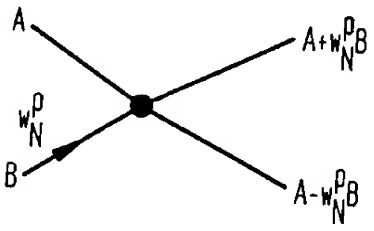


Fig 2A1

(PRIOR ART)

DIF RADIX-2 BUTTERFLY COMPUTATION

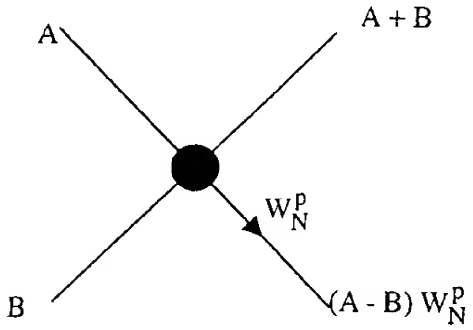


Fig 2A2

(PRIOR ART)

BUTTERFLIES REPRESENTATION OF AN 8 POINTS FFT

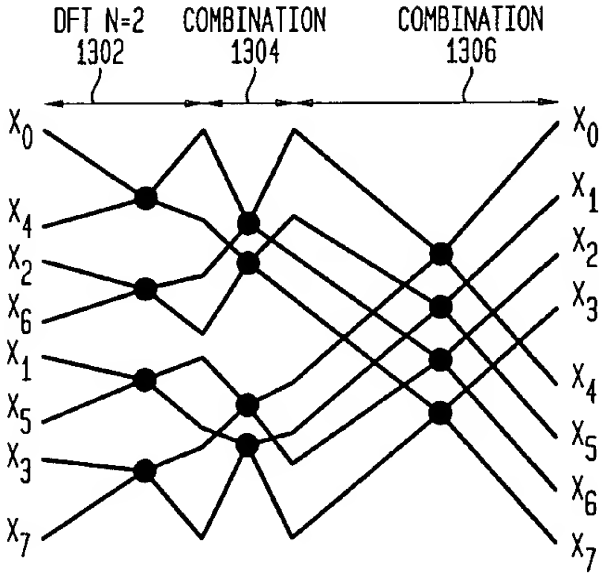


Fig 2B

FIG. 2C
(PRIOR ART)

IN PLACE FFT WITH BIT REVERSED INPUTS AND NORMALLY ORDERED OUTPUTS (r=2)

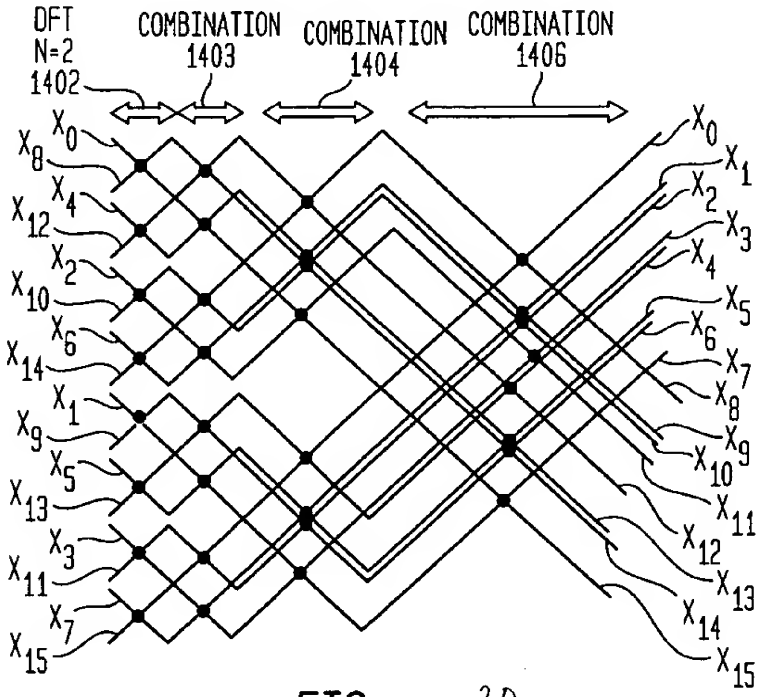


FIG. 2D
(PRIOR ART)

IN PLACE FFT WITH BIT REVERSED INPUTS AND NORMALLY ORDERED OUTPUTS

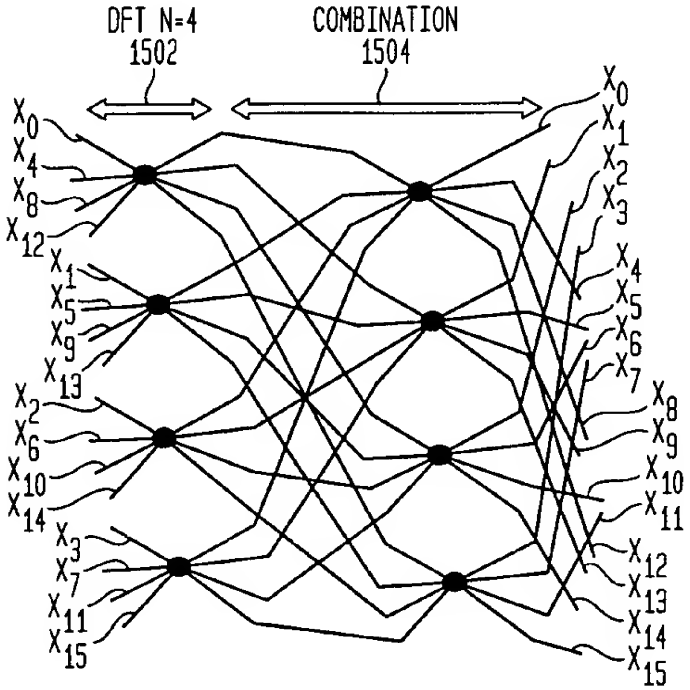


FIG. 3A

JABER'S RADIX-r DIF ENGINE

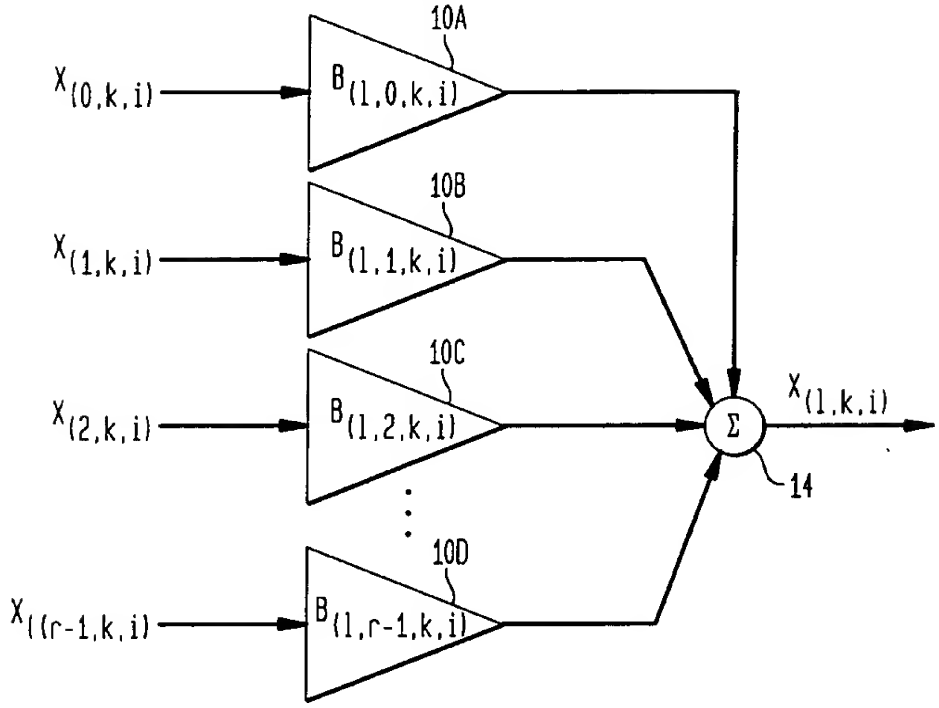


FIG. 3B

SIMPLIFIED JABER'S RADIX-r DIF ENGINE

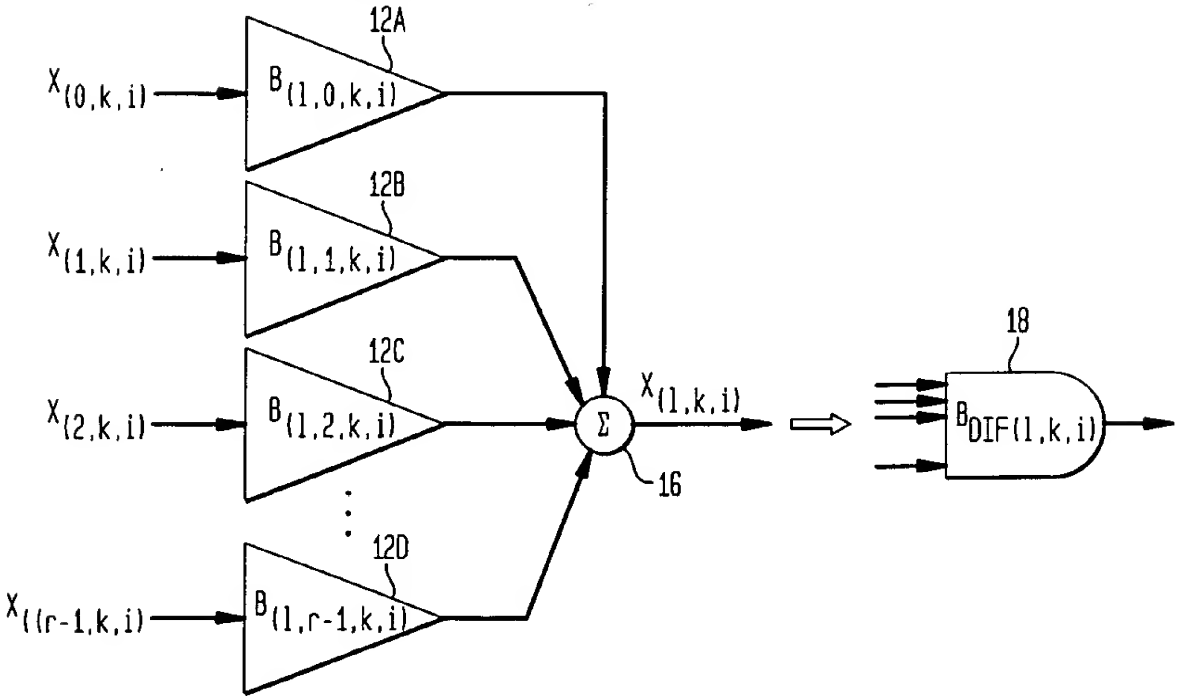


FIG. 4A

JABER'S RADIX-r DIT ENGINE

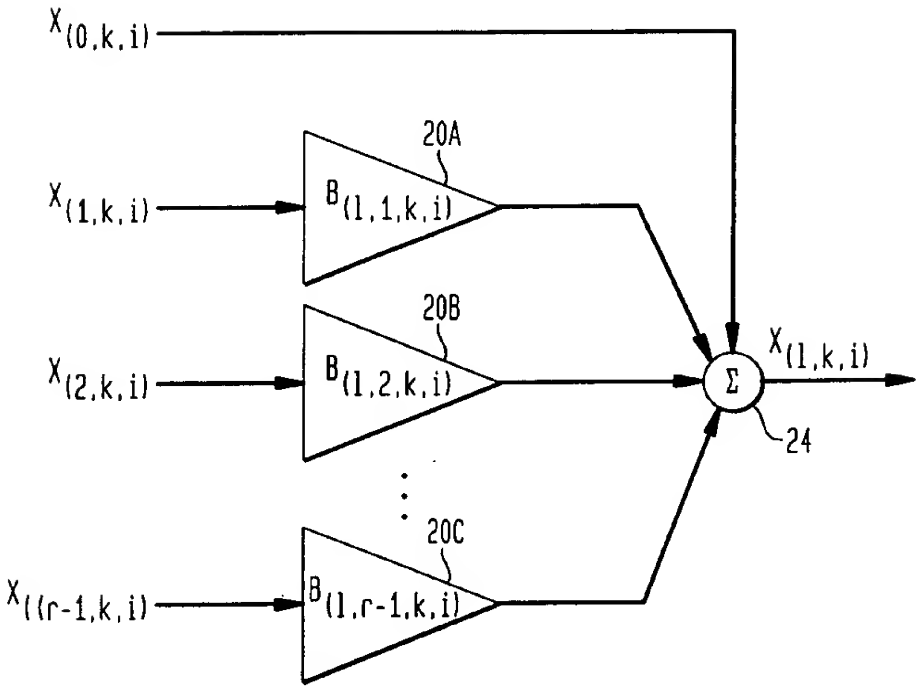


FIG. 4B

SIMPLIFIED JABER'S RADIX-r DIT ENGINE

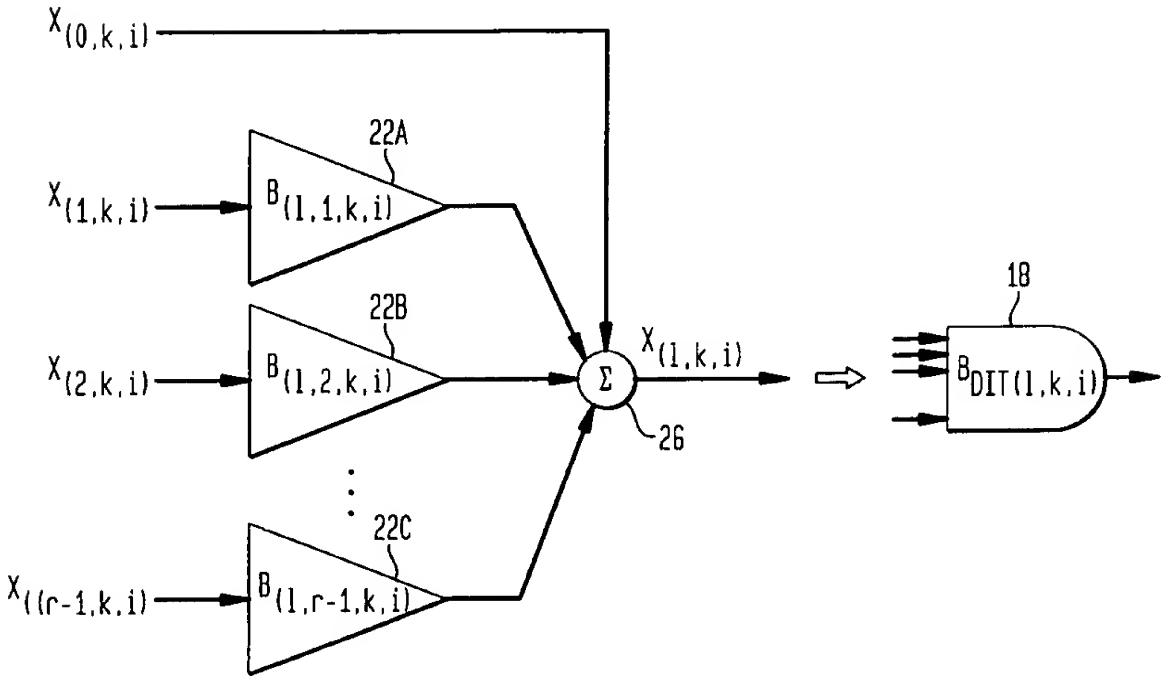


FIG. 5A

JABER'S RADIX-r DIF MODULE

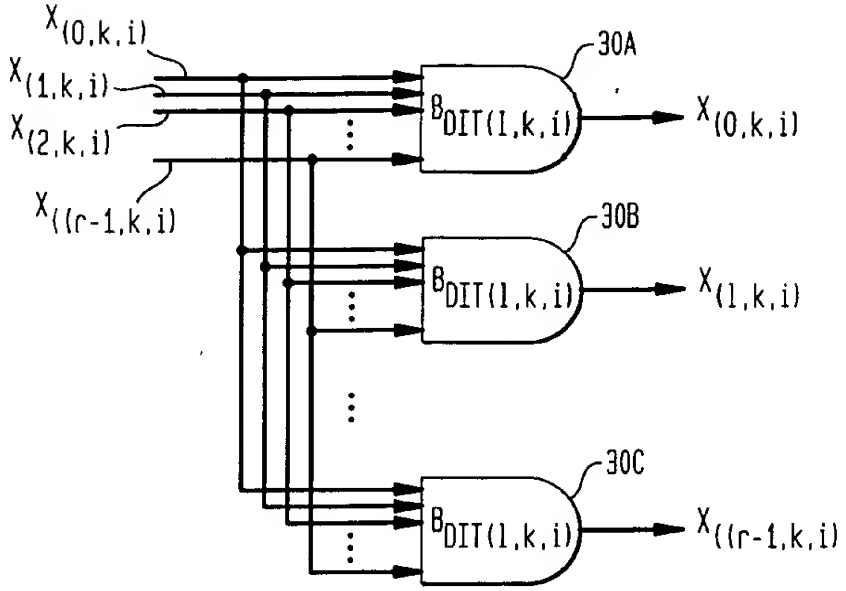


FIG. 5B

JABER'S RADIX-r DIT MODULE

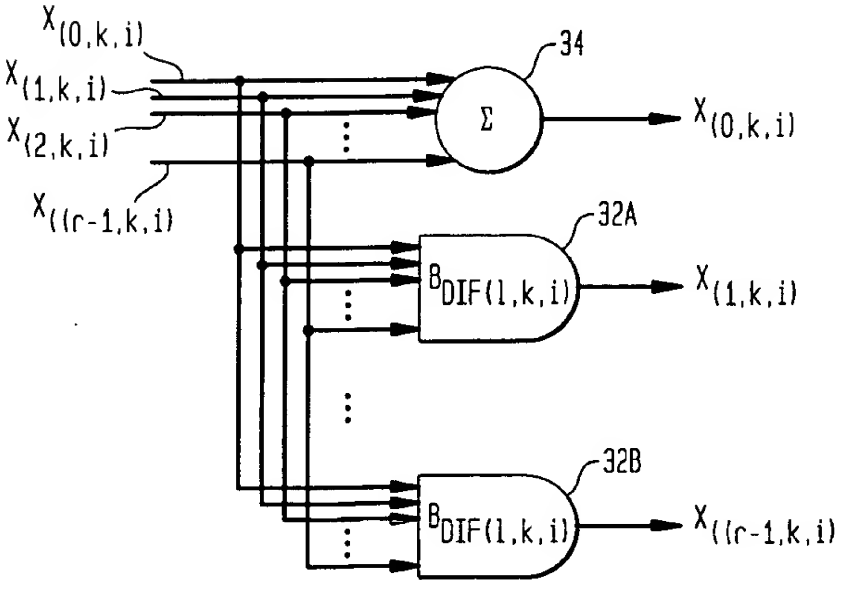


FIG. 6A

RADIX-8 DIT FFT ENGINE

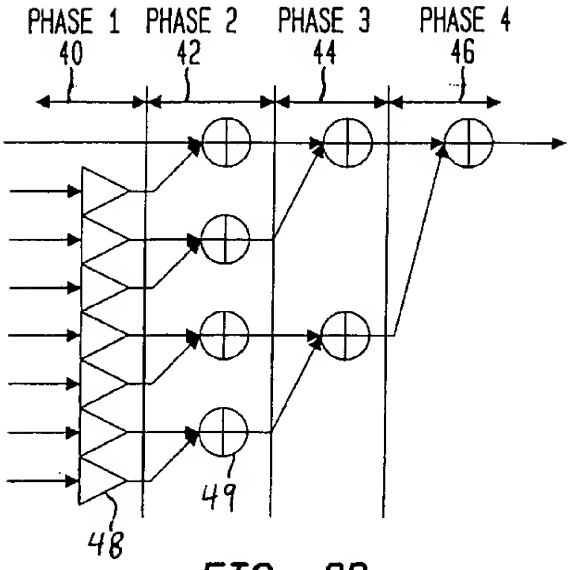
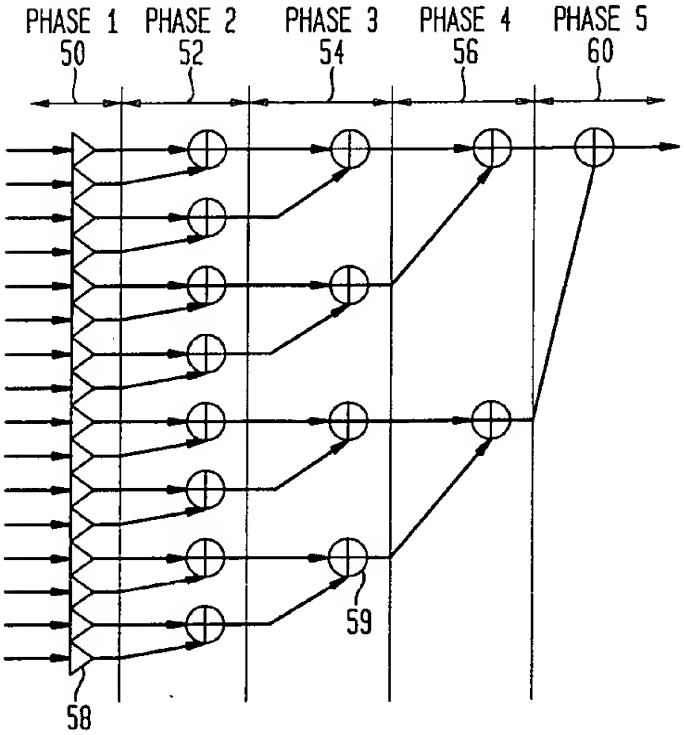


FIG. 6B

RADIX-16 DIF FFT ENGINE



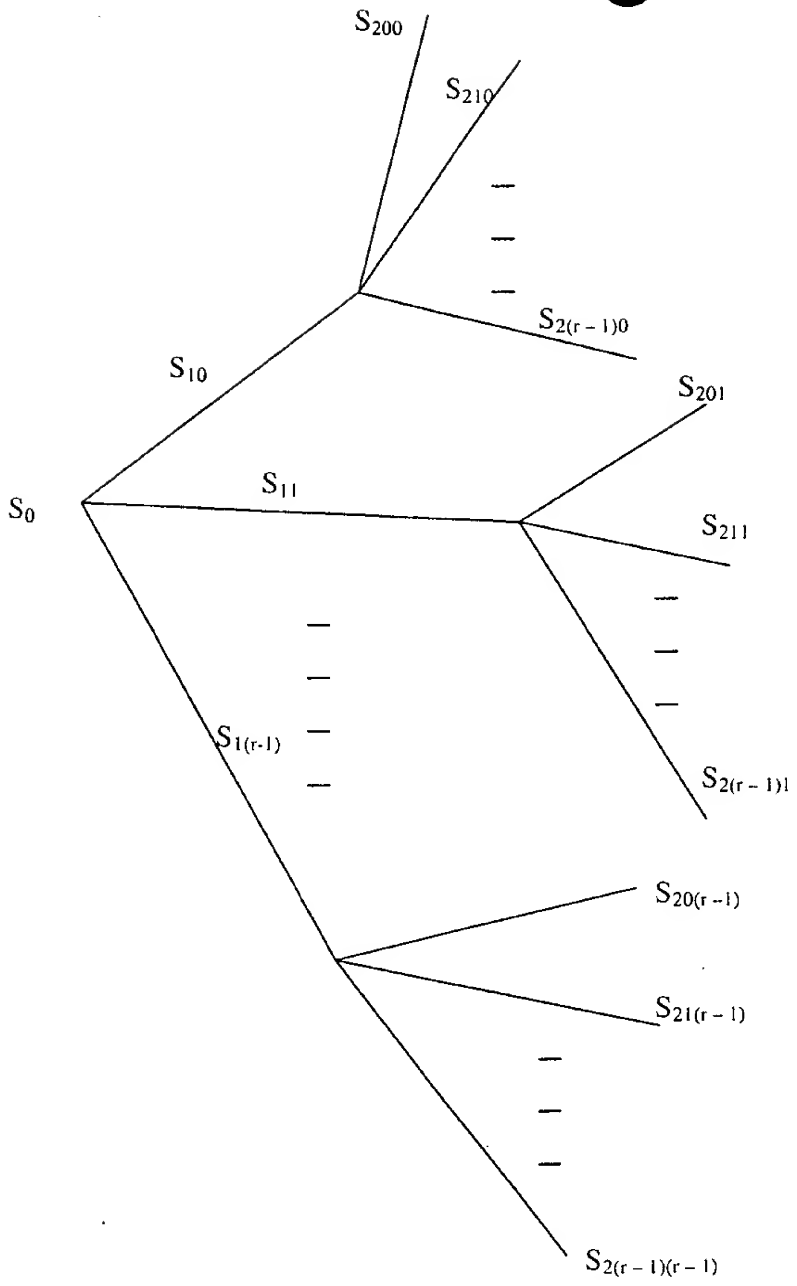

S_{200}
S_{210}
$S_{2(r-1)0}$
S_{10}
S_{201}
S_0
S_{11}
S_{211}
$S_{1(r-1)}$
$S_{2(r-1)1}$
$S_{20(r-1)}$
$S_{21(r-1)}$
$S_{2(r-1)(r-1)}$

Fig 7

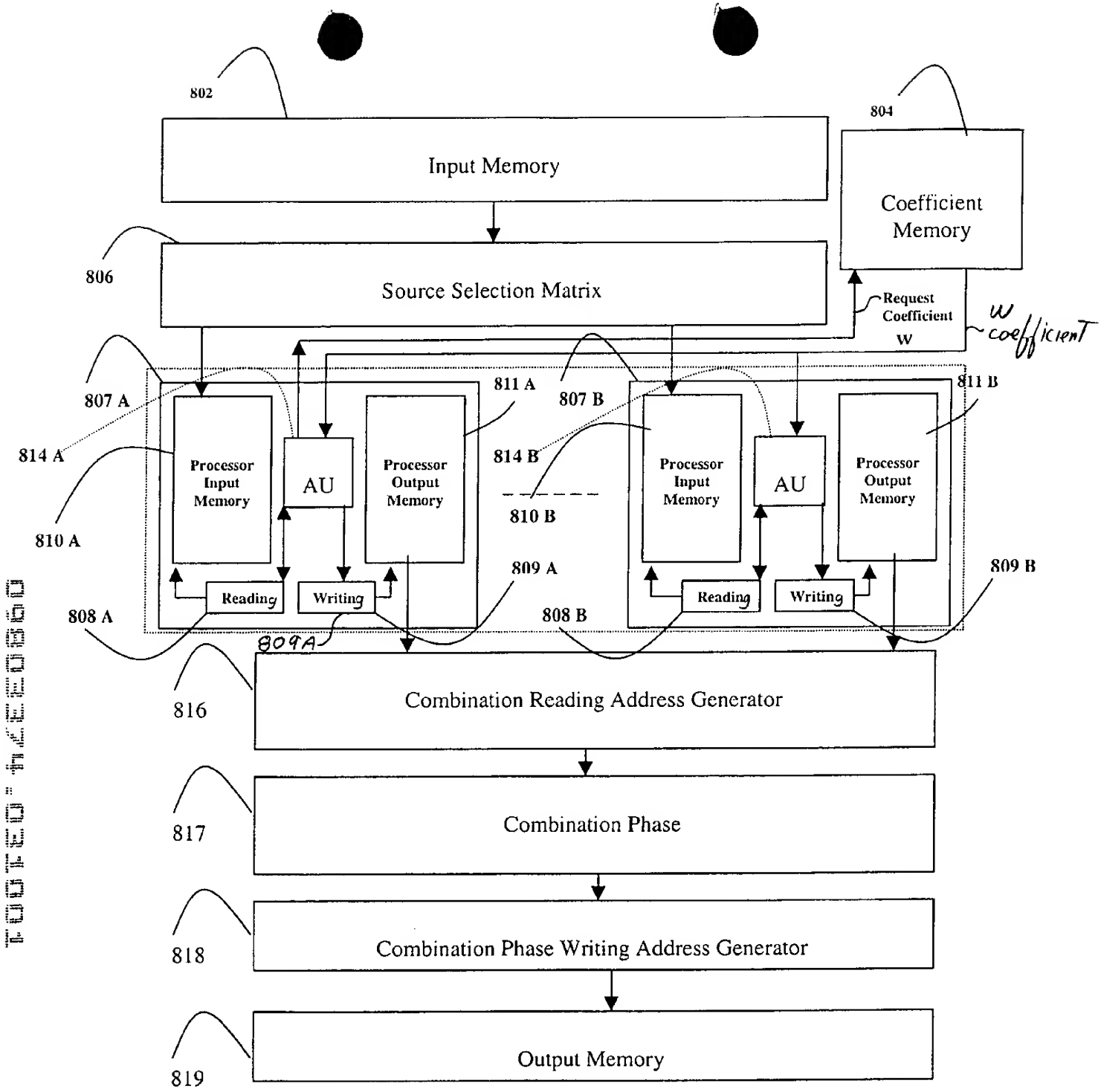

802
Input Memory
804
Coefficient Memory
806
Source Selection Matrix
Request Coefficient W
w coefficient
807 A
811 A
807 B
811 B
814 A
814 B
Processor Input Memory
AU
Processor Output Memory
Processor Input Memory
AU
Processor Output Memory
810 A
810 B
Reading
Writing
Reading
Writing
809 A
809 B
808 A
808 B
809A
816
Combination Reading Address Generator
817
Combination Phase
818
Combination Phase Writing Address Generator
819
Output Memory

Fig 8

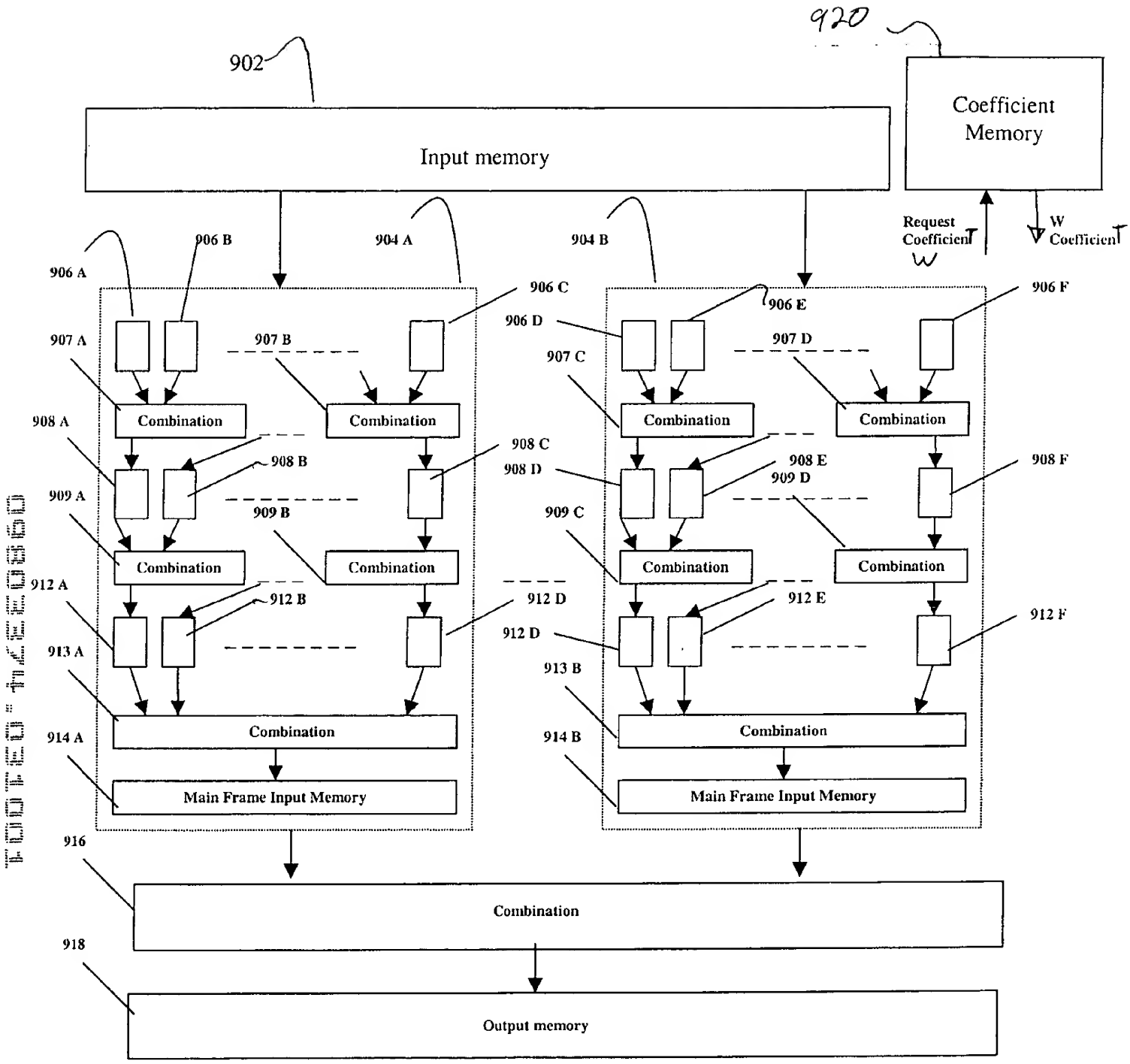
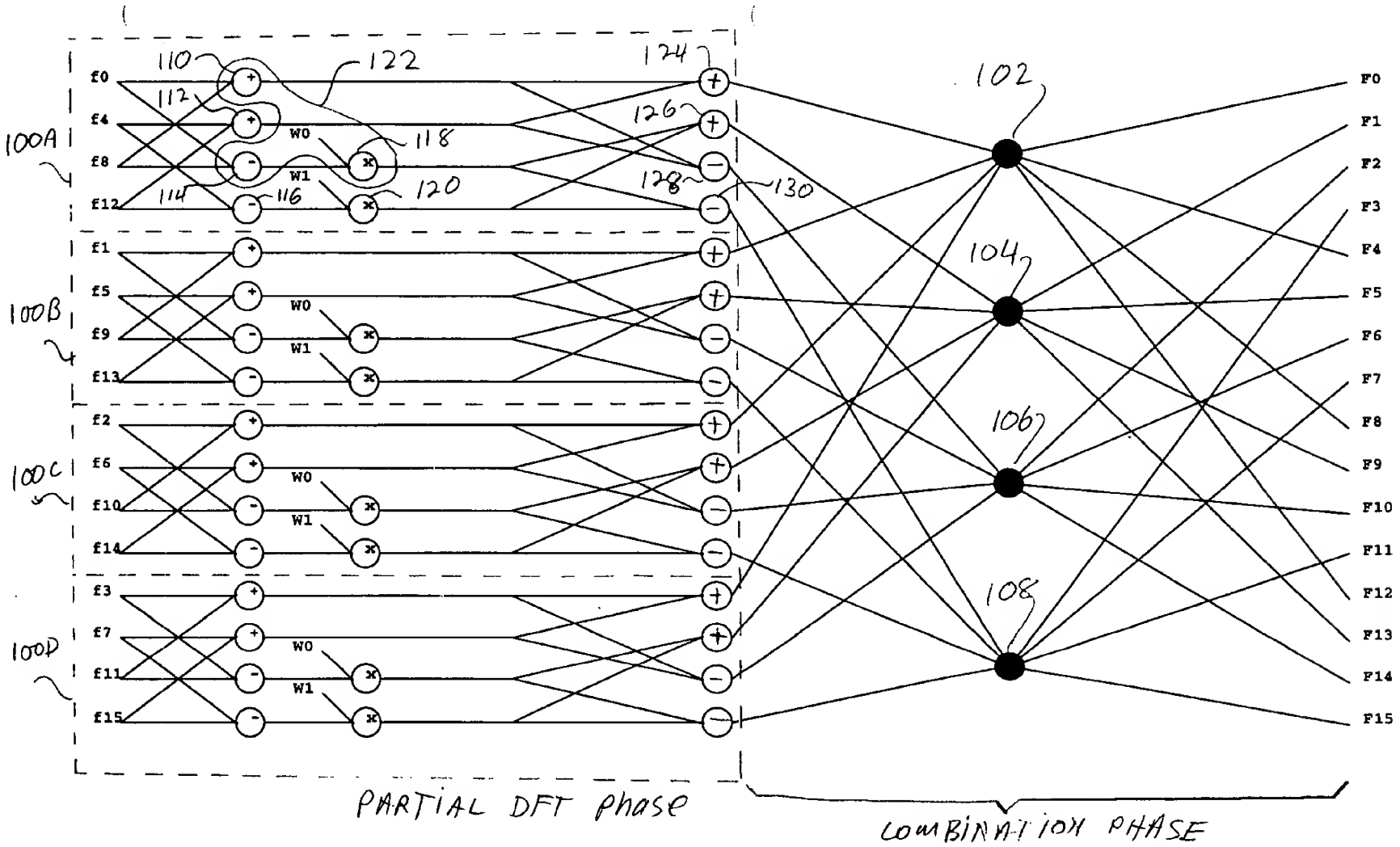
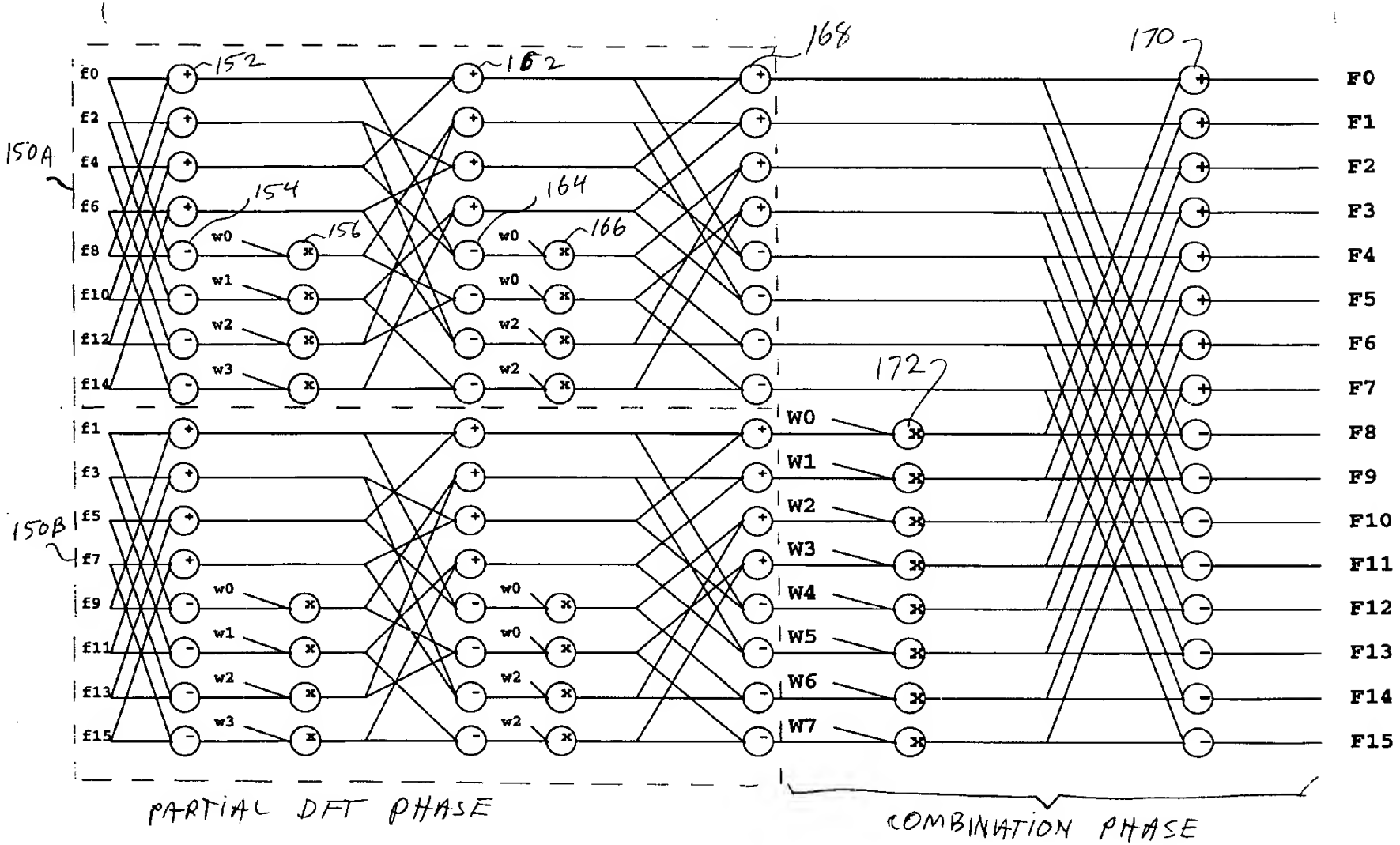

920
902
Coefficient Memory
Input memory
Request Coefficient
W Coefficient
906 A
906 B
904 A
904 B
906 C
906 D
906 E
906 F
907 A
907 B
907 C
907 D
Combination
908 A
908 B
908 C
908 D
908 E
908 F
909 A
909 B
909 C
909 D
912 A
912 B
912 D
912 E
912 F
913 A
913 B
914 A
914 B
Main Frame Input Memory
916
Combination
918
Output memory

Fig 9



16 Points FFT radix 2 on four parallel processors with combination phase

FIG 10



16 POINTS FFT MAPPING WITH COMBINATION PHASE

FIG 11